09/837734

ABSTRACT OF DISCLOSURE

A memory cell array is provided at a non-volatile semiconductor storage apparatus. In a memory cell array, the unit cell includes a memory cell field effect transistor and a select field effect transistor. The memory cell field effect transistor has a floating gate and a control gate. The select field effect transistor has a drain connected to a source of the memory cell field effect transistor. The floating gate and control gate extends to a position above a gate of the select field effect transistor.